IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered). The claims have not been amended and are provided solely for the convenience of the Examiner.

1. (PREVIOUSLY PRESENTED) A computer which processes an interrupt when an instruction in a program is executed, said computer comprising:

a data holding part which holds data at a time when said interrupt starts to occur, said data holding part holding data for continuing an interrupted instruction.

2. (ORIGINAL) The computer as claimed in claim 1, wherein said data holding part includes a plurality of registers.

3. (ORIGINAL) The computer as claimed in claim 2, said computer further comprising flags each of said flags indicating whether said data is held in said register.

4. (ORIGINAL) The computer as claimed in claim 1, said computer further comprising a data storing part, wherein said data holding part holds said data to be stored in said data storing part at a time when said interrupt occurs while a store instruction is executed, said store instruction requesting that said data is stored in said data storing part.

5. (ORIGINAL) The computer as claimed in claim 1, wherein said data holding part holds an instruction address of an instruction which causes said interrupt.

6. (CANCELLED).

7. (ORIGINAL) The computer as claimed in claim 1, wherein said data holding part holds an effective address of a load instruction or a store instruction when said interrupt occurs while said load instruction or said store instruction is executed.

8. (ORIGINAL) The computer as claimed in claim 1, wherein said data is used for recovery from said interrupt.

9. (PREVIOUSLY PRESENTED) A control method of a computer which processes an interrupt when an instruction in a program is executed, said method comprising the step of:

holding data at a time when said interrupt starts to occur, said data being used for continuing an interrupted instruction.

10. (ORIGINAL) The control method as claimed in claim 9, wherein said data is held in a plurality of registers and said data is used for recovery from a plurality of interrupts.

11. (ORIGINAL) The control method as claimed in claim 10, wherein flags are used in which each of which flags indicates whether said data is held in said register.

12. (ORIGINAL) The control method as claimed in claim 9, said control method comprising the step of:

holding said data to be stored in a data storing part in said computer at a time when said interrupt occurs while a store instruction is executed, said store instruction requesting that said data is stored in said data storing part.

13. (ORIGINAL) The control method as claimed in claim 9, said control method comprising the step of:

holding an instruction address of an instruction which causes said interrupt.

14. (CANCELLED)

15. (ORIGINAL) The control method as claimed in claim 9, said control method comprising the step of:

holding an effective address of a load instruction or a store instruction when said interrupt occurs while said load instruction or said store instruction is executed.

16. (ORIGINAL) The control method as claimed in claim 9, wherein said data is used for recovery from said interrupt.

REMARKS

Rejections under 35 U.S.C. § 102(e)

In the February 28, 2005 Office Action, the Examiner indicated that claims 1-5, 7-13, 15 and 16 were pending and rejected under 35 U.S.C. § 102(e) as being anticipated by Miyake et al. (Pub. No. US 2001/0004757) (hereafter, "Miyake '757"). The rejections are respectfully traversed. No changes have been made to the claims and thus, claims 1-5, 7-13, 15, and 16 are pending and under consideration.

The provisions of 35 U.S.C. 102(e) require "an application for patent, published under section 122(b), by **another** ...," but Miyake '757 has the same inventive entity as the subject U.S. application being examined. Therefore, Miyake '757 is not a prior art reference under 35 U.S.C. 102(e). It is respectfully requested that the final Rejection be withdrawn.

Conclusion

For the reasons set forth above, withdrawal of the final rejection is respectfully requested. There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 6/28/05

By: Richard A. Gollhofer

Richard A. Gollhofer
Registration No. 31,106

CERTIFICATE UNDER 37 CFR 1.8(a)
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
on JUNE 28, 2005
STAAS & HALSEY
By: JOAN L. YOUNG
Date: 6-28-2005

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501